FIG . 1

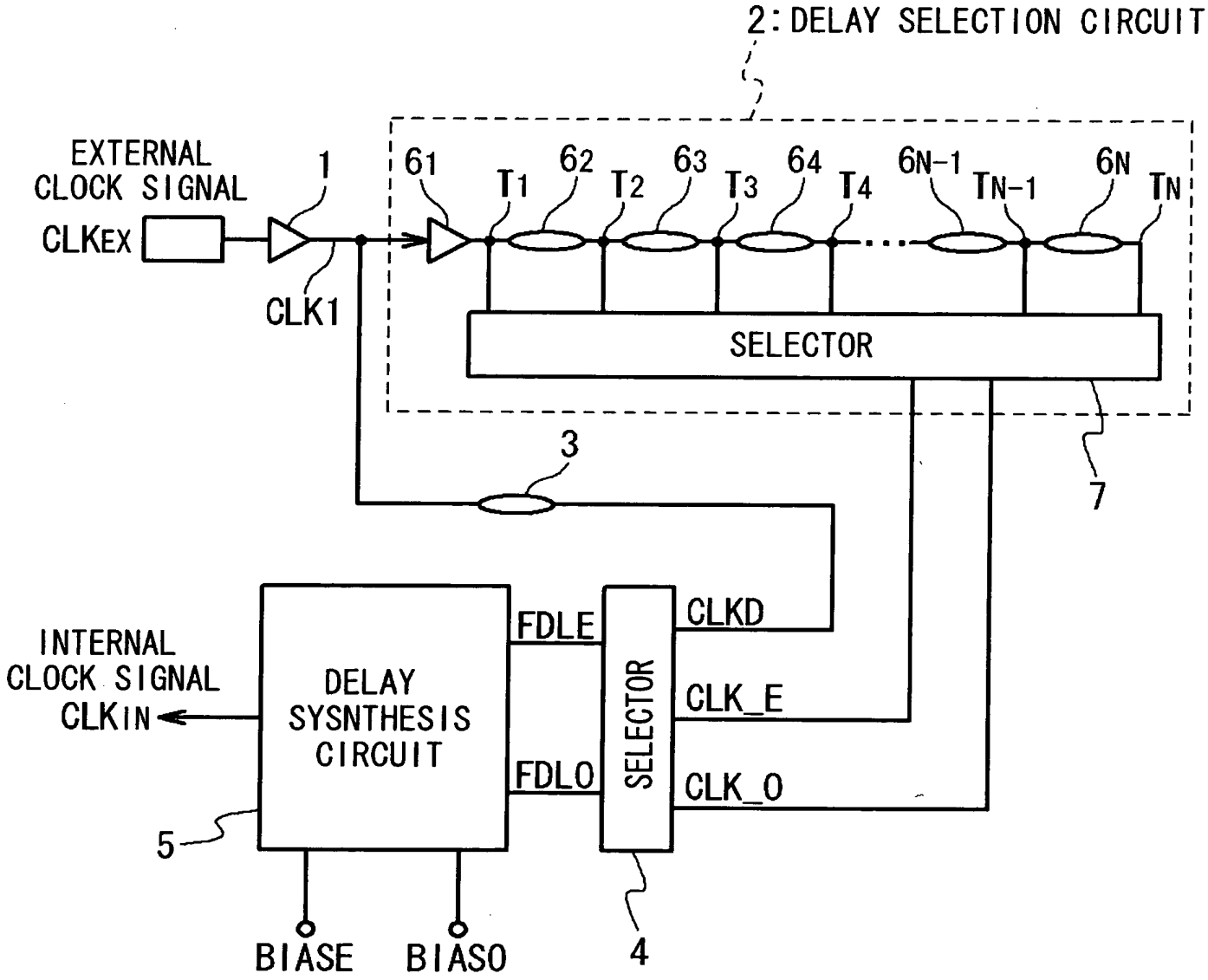
2: DELAY SELECTION CIRCUIT
EXTERNAL CLOCK SIGNAL
CLKEX
1
CLK1
61
T1
62
T2
63
T3
64
T4
6N-1
TN-1
6N
TN
SELECTOR
7
3
INTERNAL CLOCK SIGNAL
CLKIN
DELAY SYSNTHESIS CIRCUIT
5
FDLE
FDLO
SELECTOR
CLKD
CLK_E
CLK_O
4
BIASE
BIASO

FIG . 2

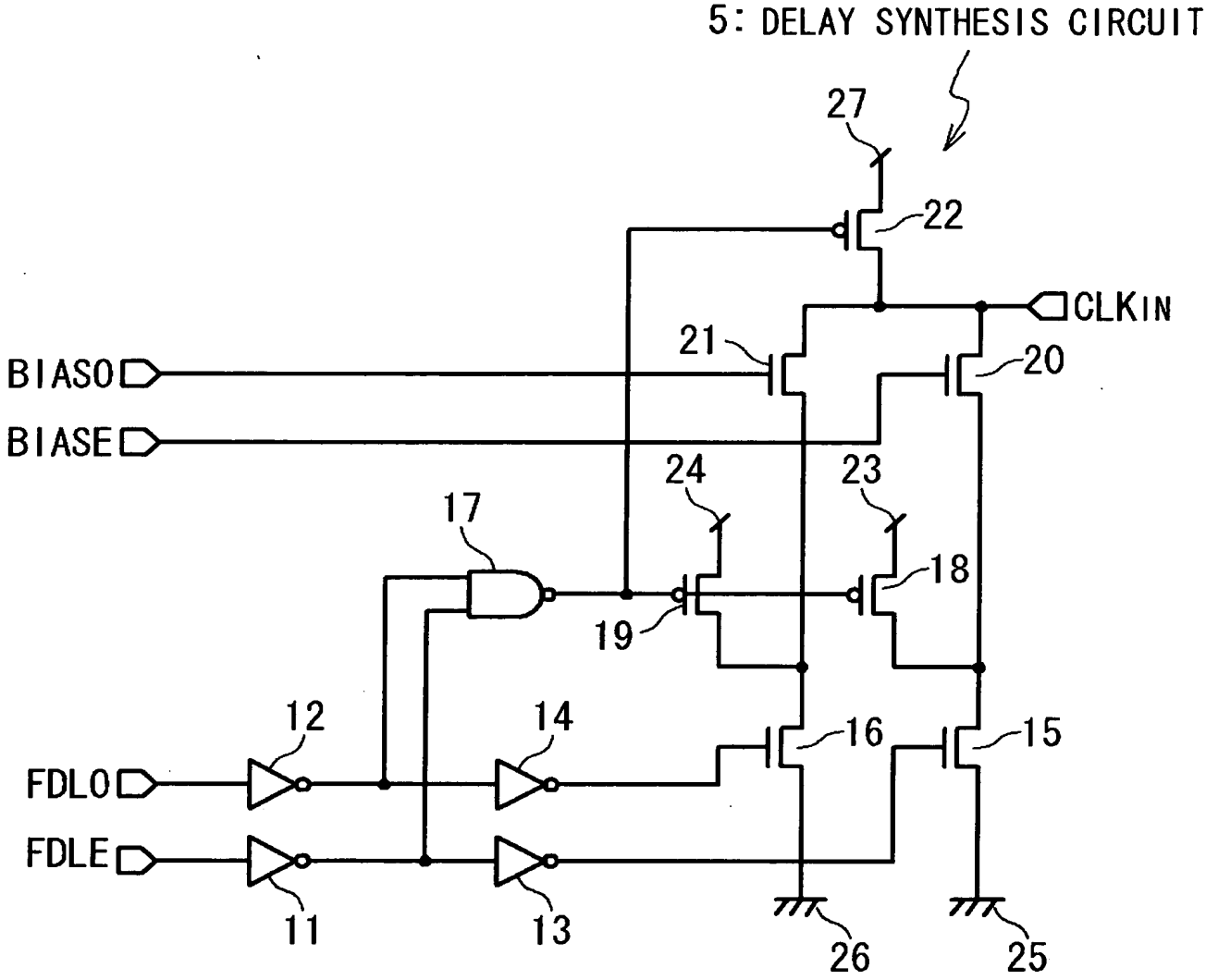
5: DELAY SYNTHESIS CIRCUIT
27
22
CLKIN
21
20
BIASO
BIASE
24
23
17
18
19
12
14
16
15
FDLO
FDLE
11
13
26
25

FIG . 3

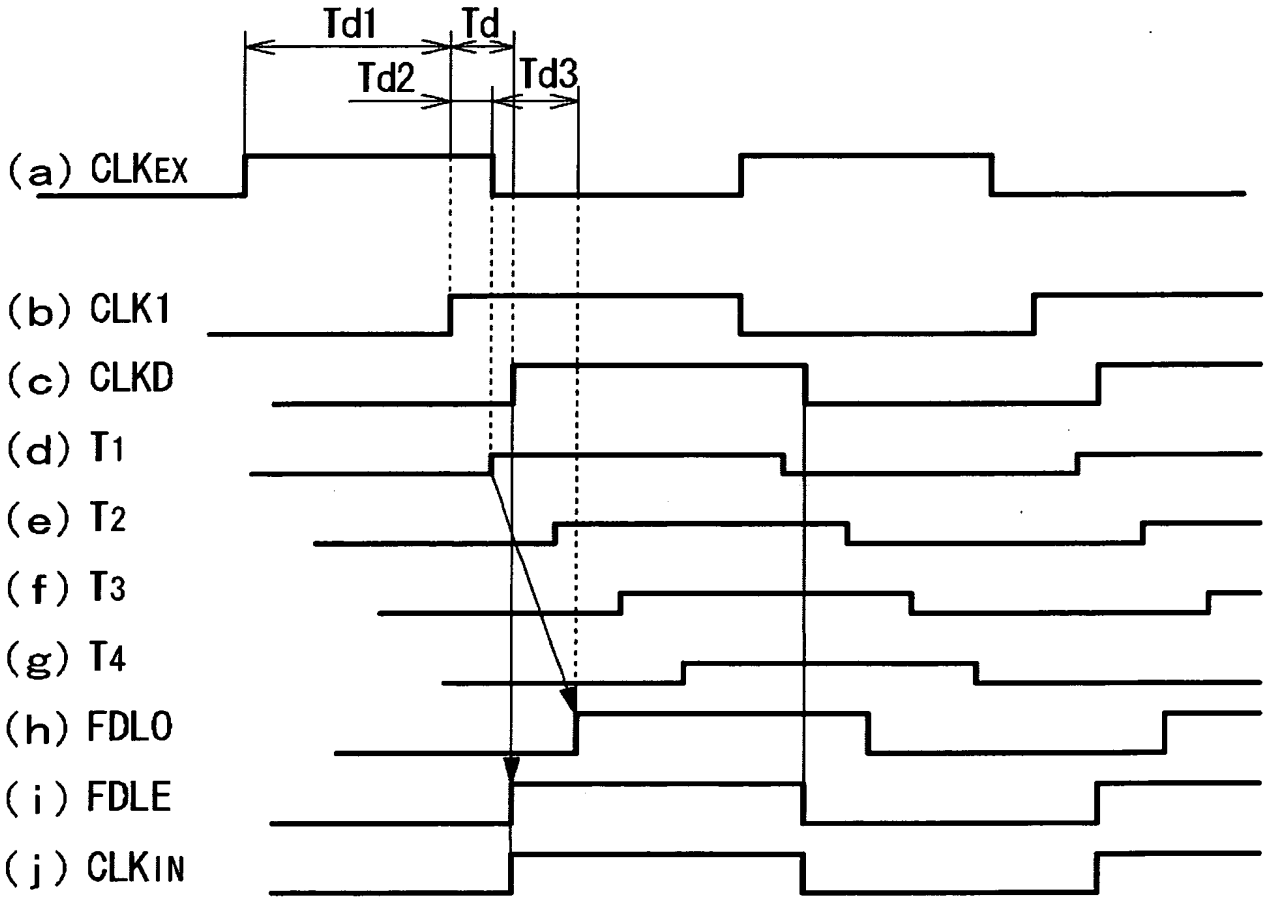
Td1
Td
Td2
Td3
(a) CLKEX
(b) CLK1
(c) CLKD
(d) T1
(e) T2
(f) T3
(g) T4
(h) FDLO
(i) FDLE
(j) CLKIN

FIG . 4

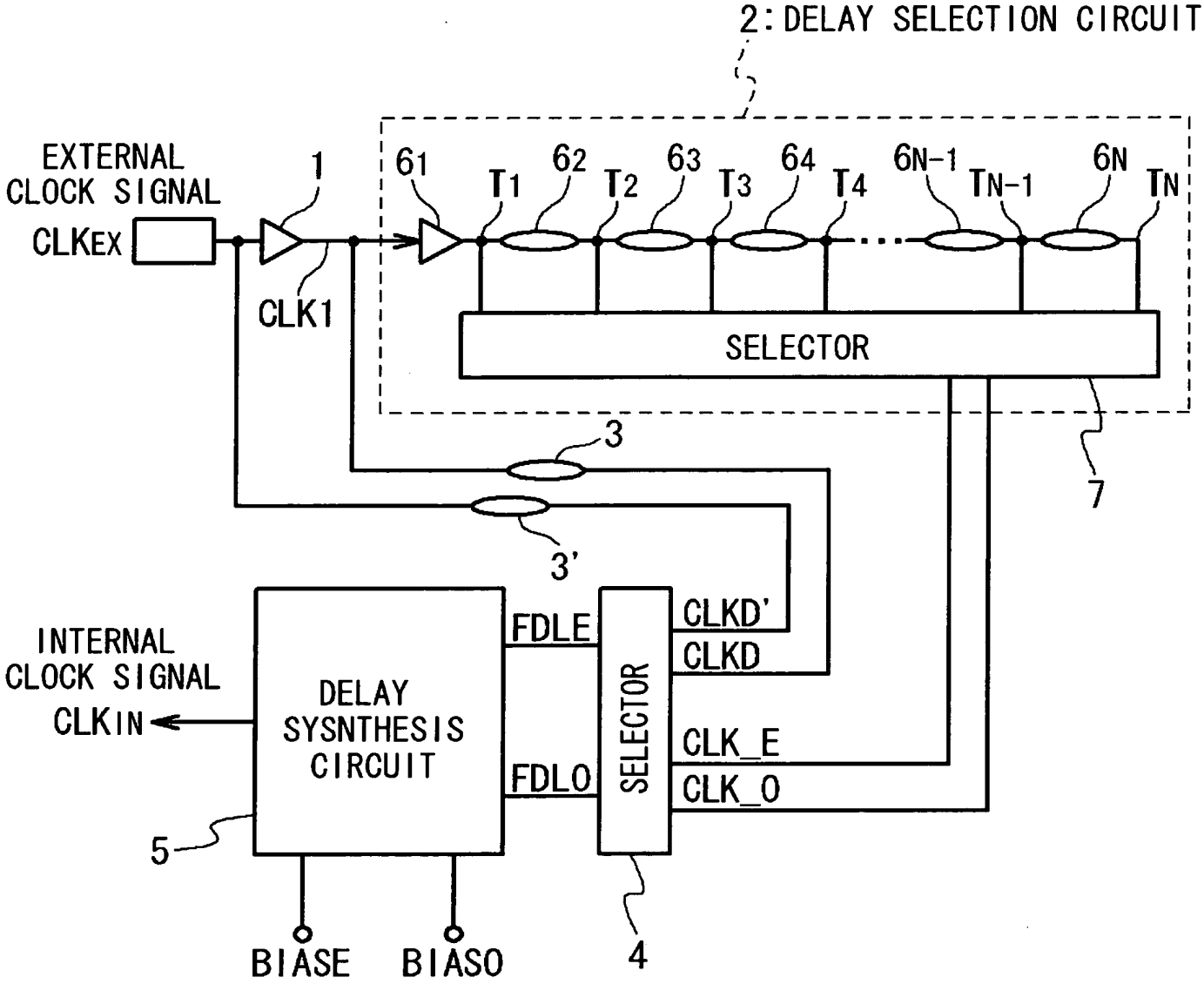
2: DELAY SELECTION CIRCUIT
EXTERNAL CLOCK SIGNAL
CLKEX
1
CLK1
61
T1
62
T2
63
T3
64
T4
6N-1
TN-1
6N
TN
SELECTOR
7
3
3'
INTERNAL CLOCK SIGNAL
CLKIN
DELAY SYSNTHESIS CIRCUIT
5
FDLE
FDLO
SELECTOR
CLKD'
CLKD
CLK_E
CLK_O
4
BIASE
BIASO

FIG . 5

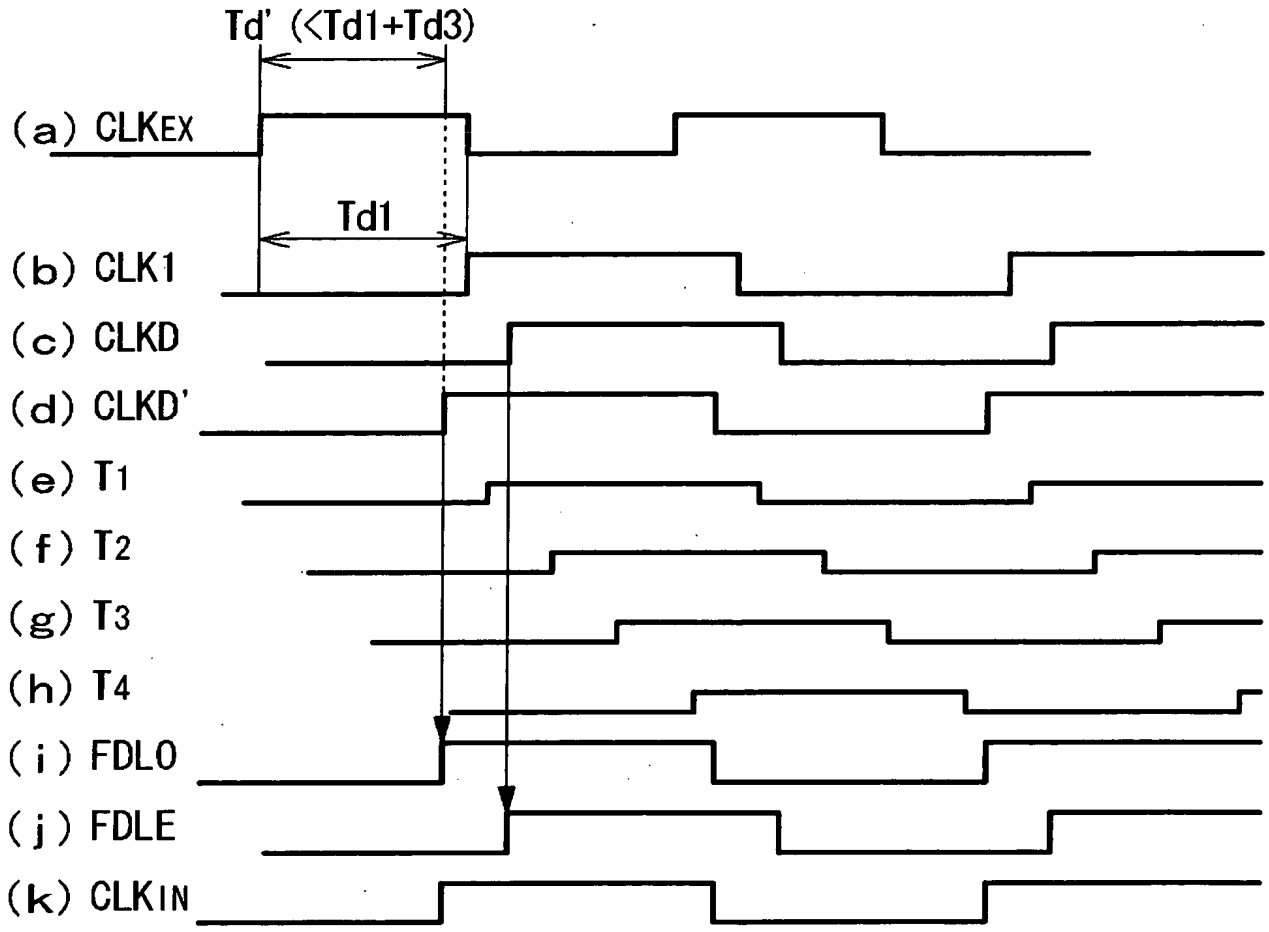
Td' (<Td1+Td3)
(a) CLKEX
Td1
(b) CLK1
(c) CLKD
(d) CLKD'
(e) T1
(f) T2
(g) T3
(h) T4
(i) FDLO
(j) FDLE
(k) CLKIN

FIG . 6

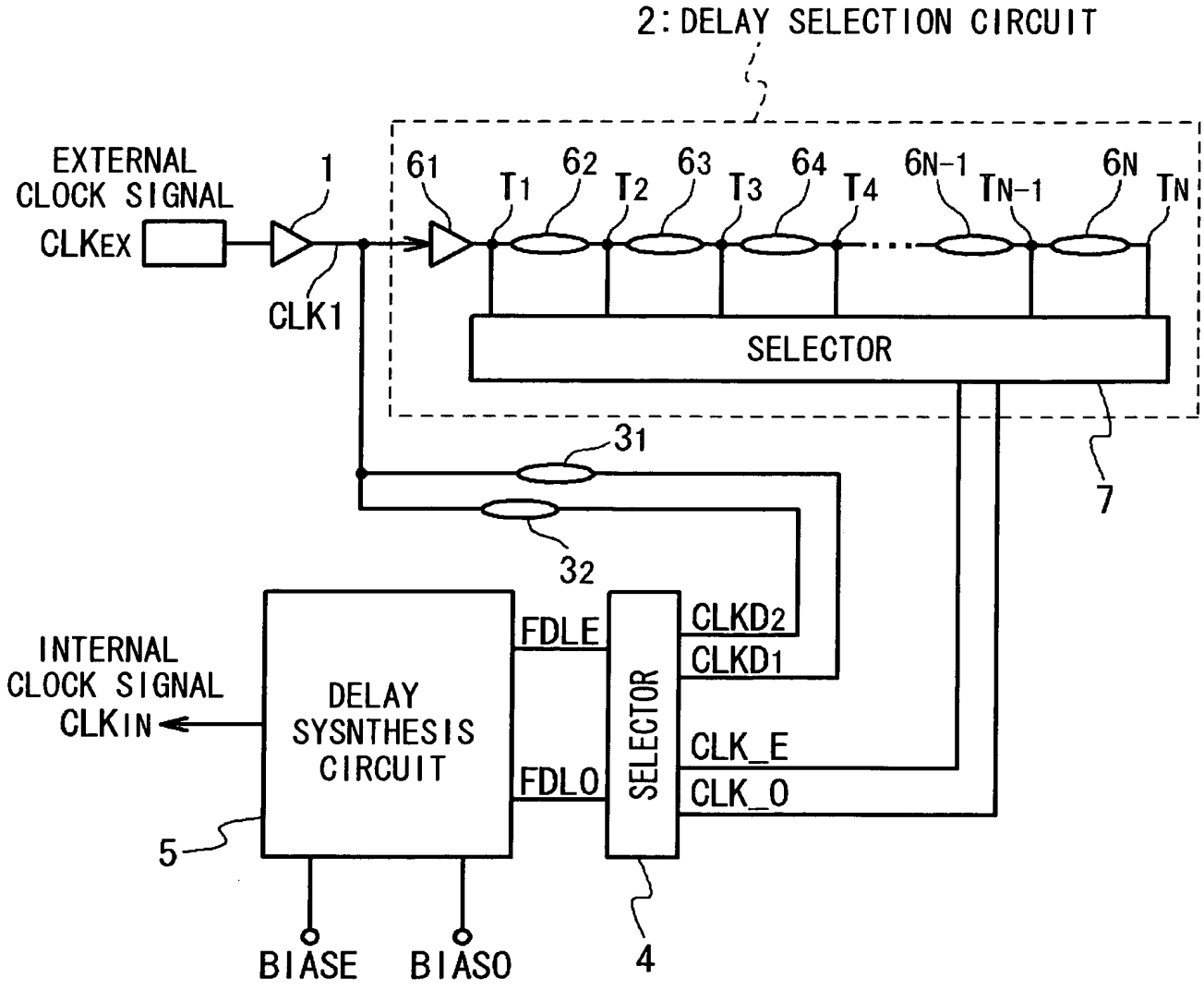
2: DELAY SELECTION CIRCUIT
EXTERNAL CLOCK SIGNAL
CLKEX
1
CLK1
61
T1
62
T2
63
T3
64
T4
6N-1
TN-1
6N
TN
SELECTOR
7
31
32
INTERNAL CLOCK SIGNAL
CLKIN
DELAY SYSNTHESIS CIRCUIT
5
FDLE
FDLO
SELECTOR
CLKD2
CLKD1
CLK_E
CLK_O
4
BIASE
BIASO

FIG . 7

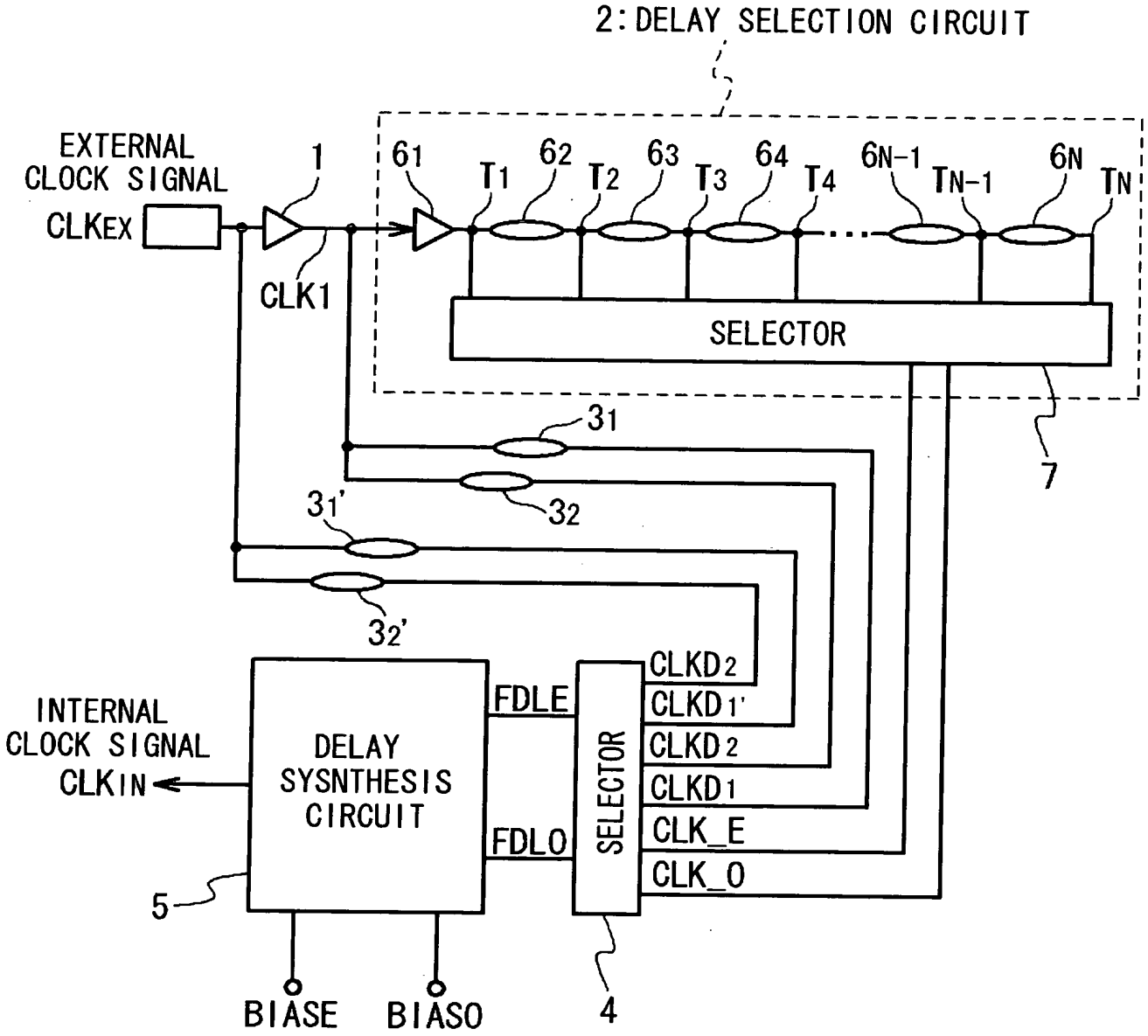
2: DELAY SELECTION CIRCUIT
EXTERNAL CLOCK SIGNAL
CLKEX
1
CLK1
61
T1
62
T2
63
T3
64
T4
6N-1
TN-1
6N
TN
SELECTOR
7
31
32
31'
32'
INTERNAL CLOCK SIGNAL
CLKIN
DELAY SYSNTHESIS CIRCUIT
5
FDLE
FDLO
SELECTOR
4
CLKD2
CLKD1'
CLKD2
CLKD1
CLK_E
CLK_O
BIASE
BIASO

FIG . 8 PRIOR ART

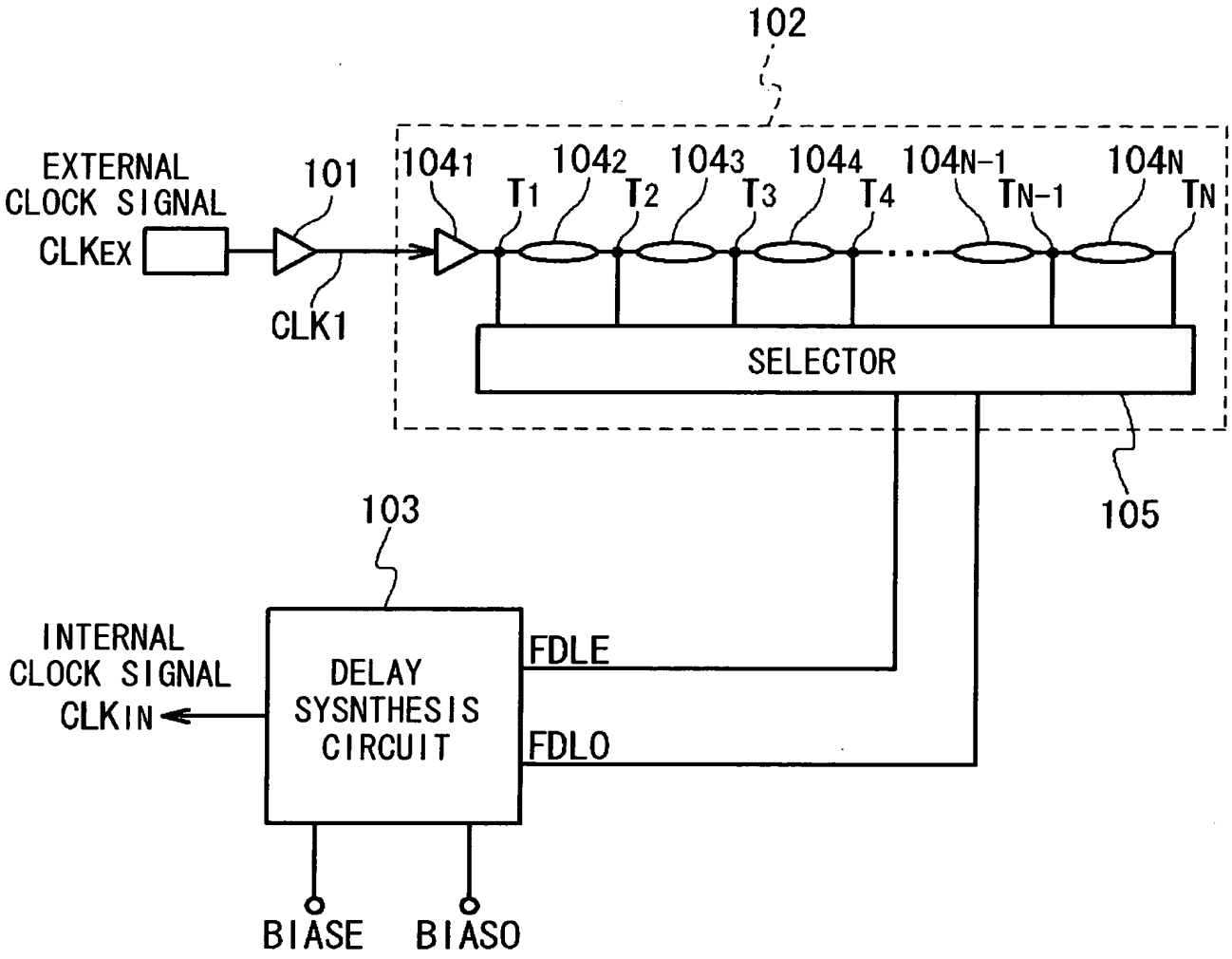

FIG . 9 PRIOR ART